FIG. 1

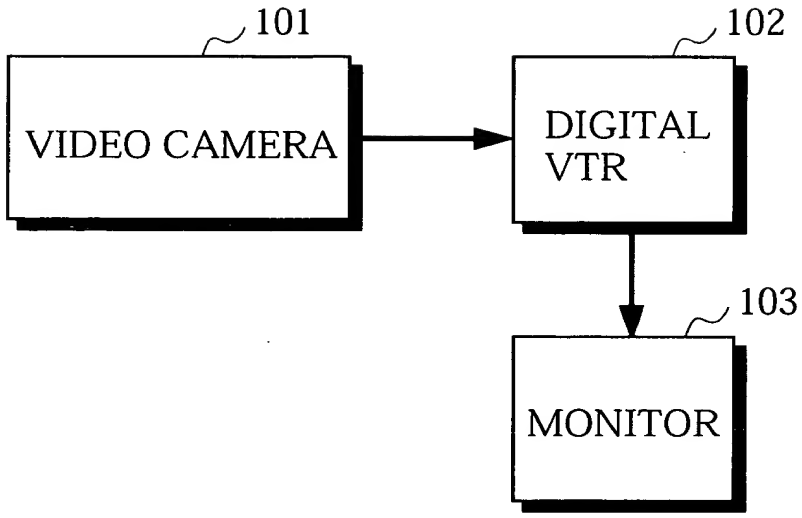


FIG. 2

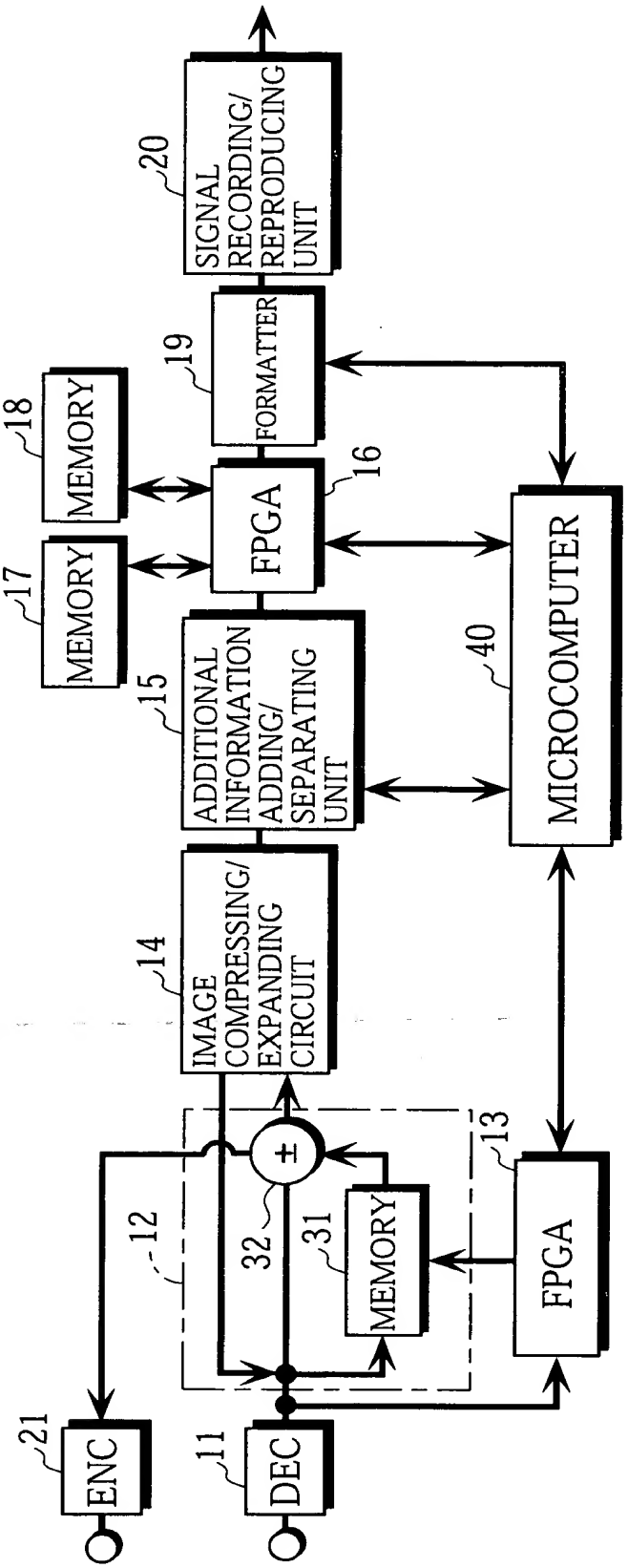

20
SIGNAL RECORDING/ REPRODUCING UNIT
19
FORMATTER
18
MEMORY
17
MEMORY
16
FPGA
15
ADDITIONAL INFORMATION ADDING/ SEPARATING UNIT
40
MICROCOMPUTER
14
IMAGE COMPRESSING/ EXPANDING CIRCUIT
13
12
32
31
MEMORY
FPGA
21
ENC
11
DEC

FIG. 3

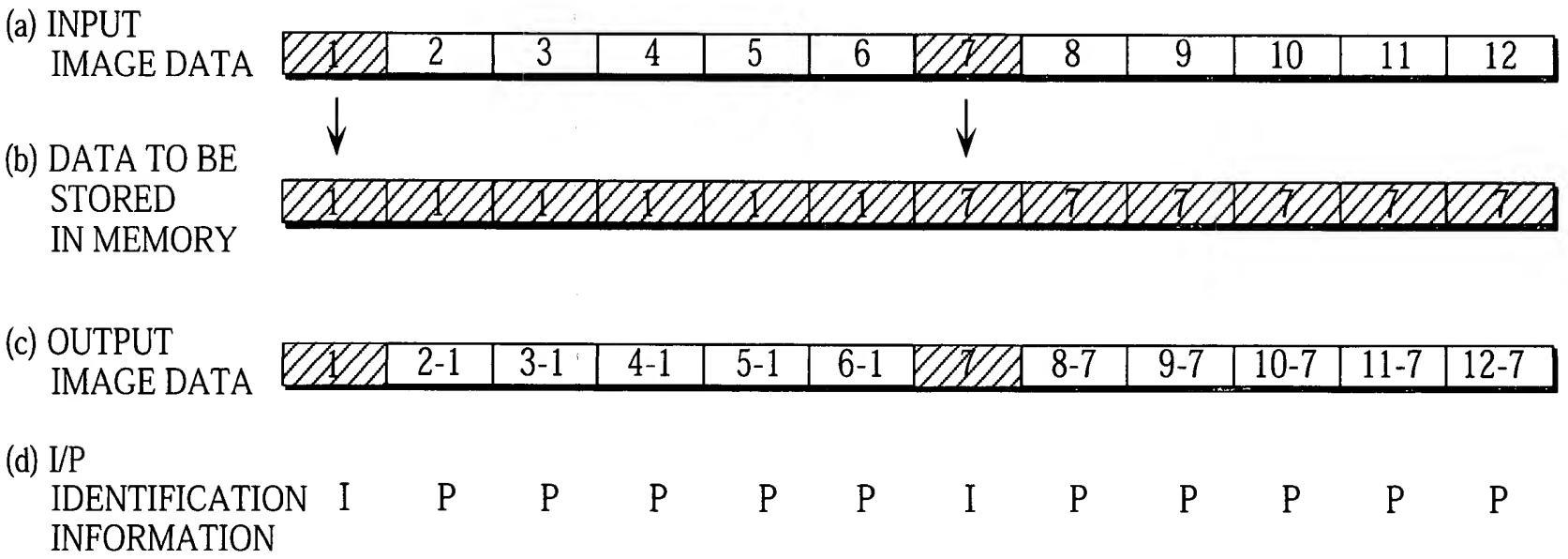

(a) INPUT IMAGE DATA
1
2
3
4
5
6
7
8
9
10
11
12
(b) DATA TO BE STORED IN MEMORY
(c) OUTPUT IMAGE DATA
1
2-1
3-1
4-1
5-1
6-1
7
8-7
9-7
10-7
11-7
12-7
(d) I/P IDENTIFICATION INFORMATION
I P P P P P I P P P P P

FIG. 4

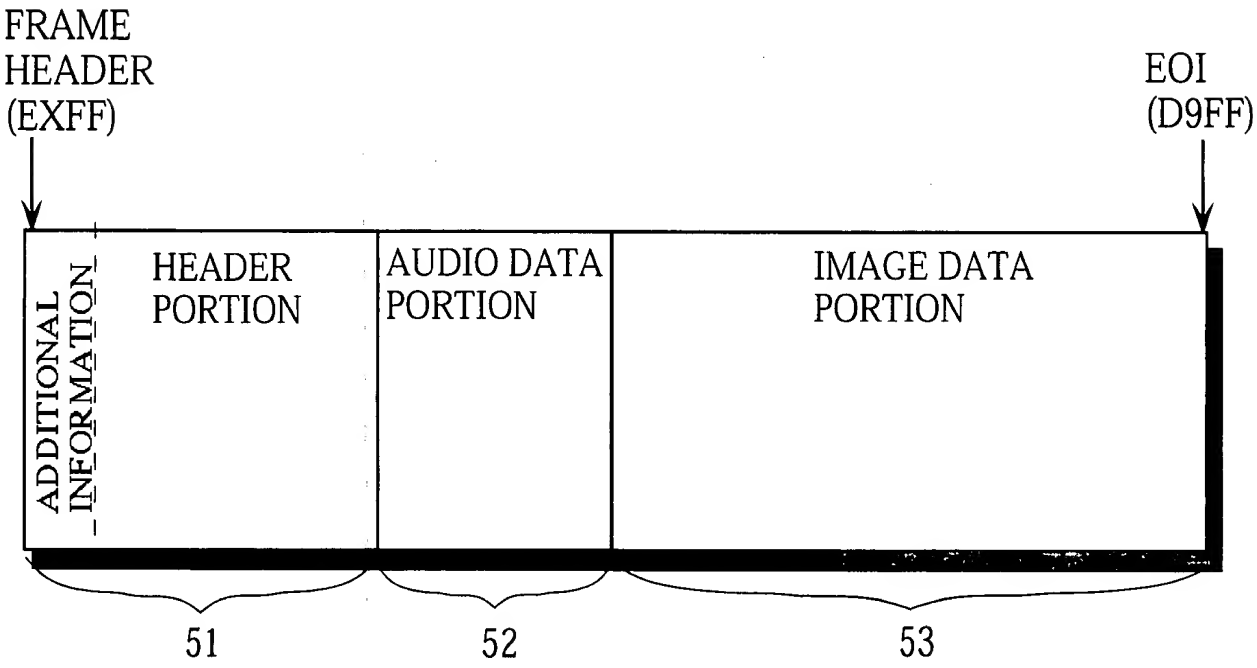

FRAME
HEADER
(EXFF)
EOI
(D9FF)
ADDITIONAL INFORMATION
HEADER PORTION
AUDIO DATA PORTION
IMAGE DATA PORTION
51
52
53

FIG. 5

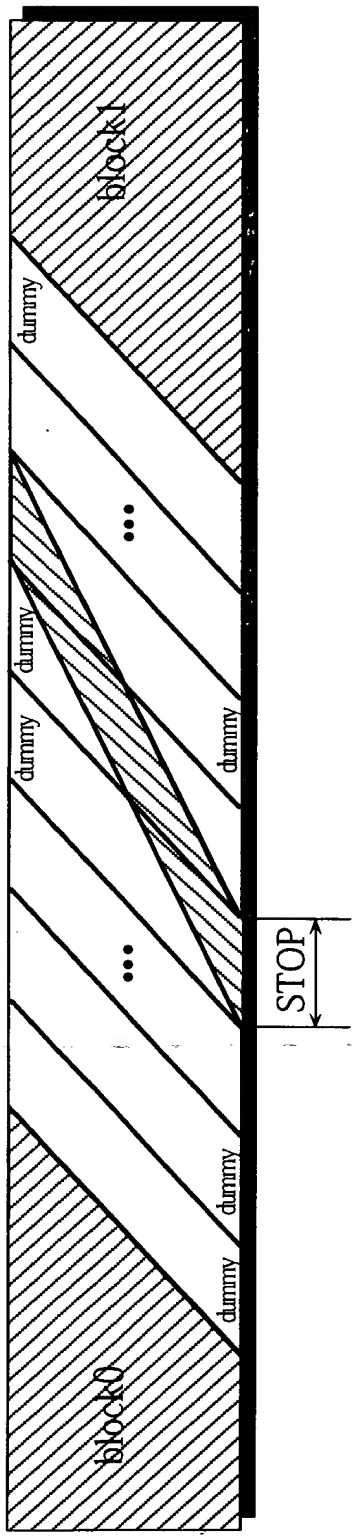


FIG. 6

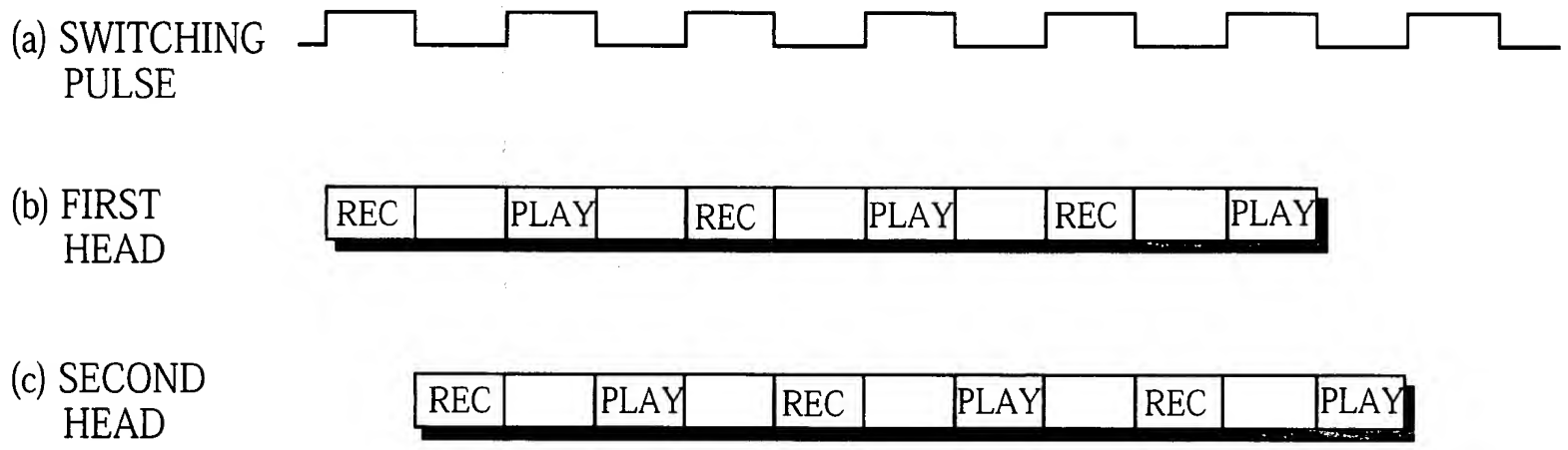

(a) SWITCHING PULSE
(b) FIRST HEAD
REC
PLAY
REC
PLAY
REC
PLAY
(c) SECOND HEAD
REC
PLAY
REC
PLAY
REC
PLAY

FIG. 7

INDEX	ADDRESS IN WHICH FRAME HEADER IS STORED
1	xxxxh
2	xxxxh
3	xxxxh
4	xxxxh
	xxxxh
	xxxxh
	xxxxh
	xxxxh
	xxxxh
	xxxxh
2024	xxxxh

FIG. 8

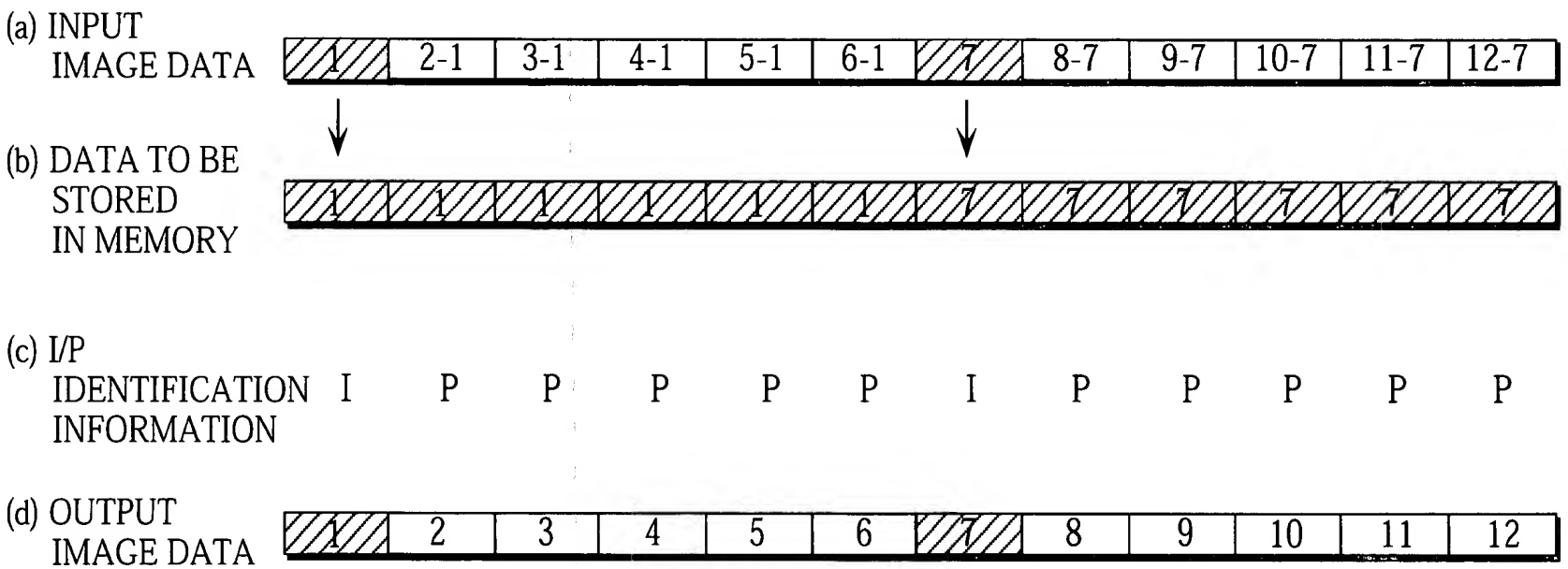

(a) INPUT IMAGE DATA
1
2-1
3-1
4-1
5-1
6-1
7
8-7
9-7
10-7
11-7
12-7
(b) DATA TO BE STORED IN MEMORY
1
1
1
1
1
1
7
7
7
7
7
7
(c) I/P IDENTIFICATION INFORMATION
I P P P P P I P P P P P
(d) OUTPUT IMAGE DATA
1
2
3
4
5
6
7
8
9
10
11
12

FIG. 9

INDEX NUMBER IN SUB-BANK	STORED DATA
1	I1
2	P11
3	P12
4	P13
5	I2
6	P21
7	P22
8	P23
9	I3
10	P31
11	P32
12	P33

FIG. 10

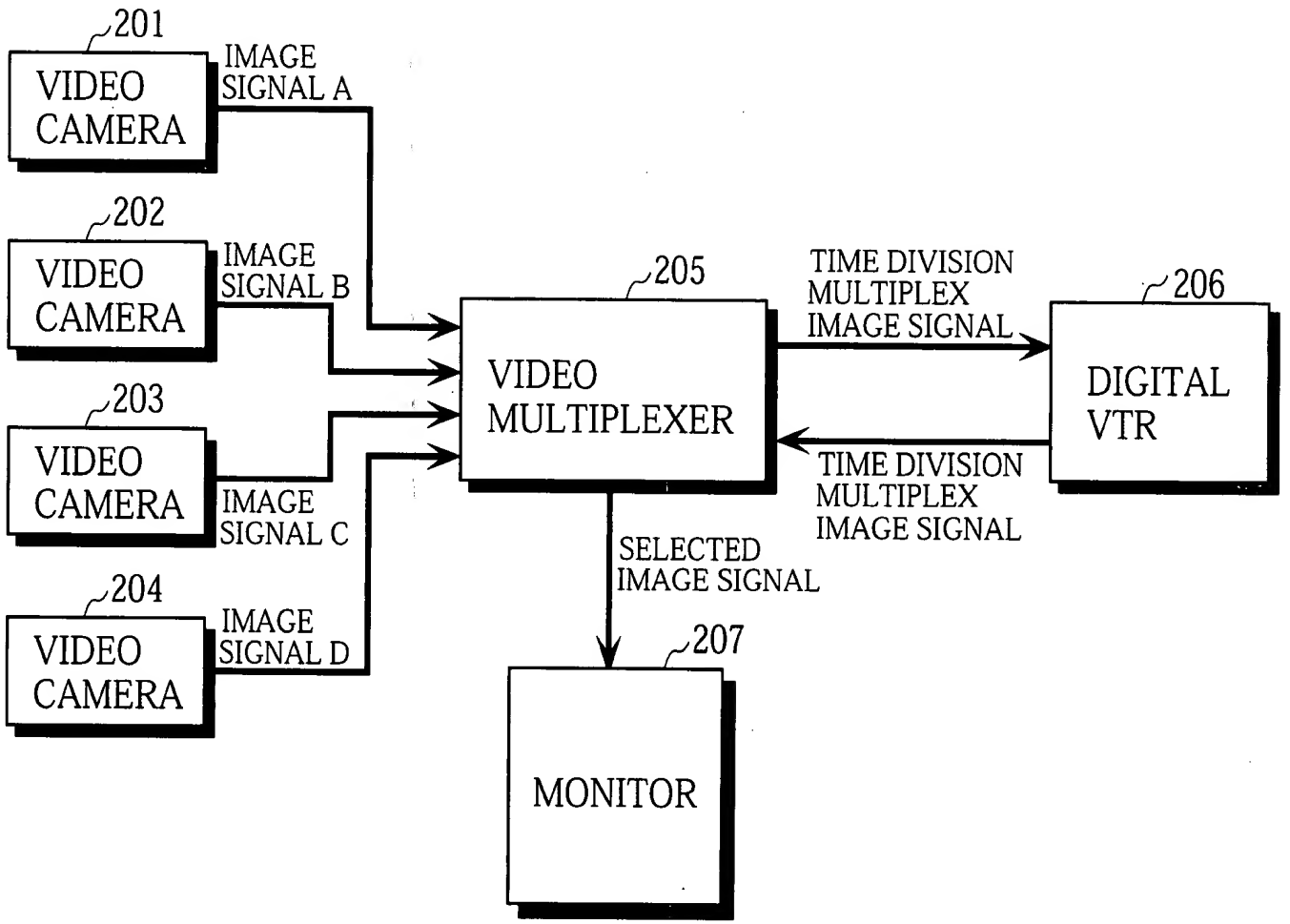

201
VIDEO CAMERA
IMAGE SIGNAL A
202
VIDEO CAMERA
IMAGE SIGNAL B
203
VIDEO CAMERA
IMAGE SIGNAL C
204
VIDEO CAMERA
IMAGE SIGNAL D
205
VIDEO MULTIPLEXER
TIME DIVISION MULTIPLEX IMAGE SIGNAL
206
DIGITAL VTR
TIME DIVISION MULTIPLEX IMAGE SIGNAL
SELECTED IMAGE SIGNAL
207
MONITOR

FIG. 11

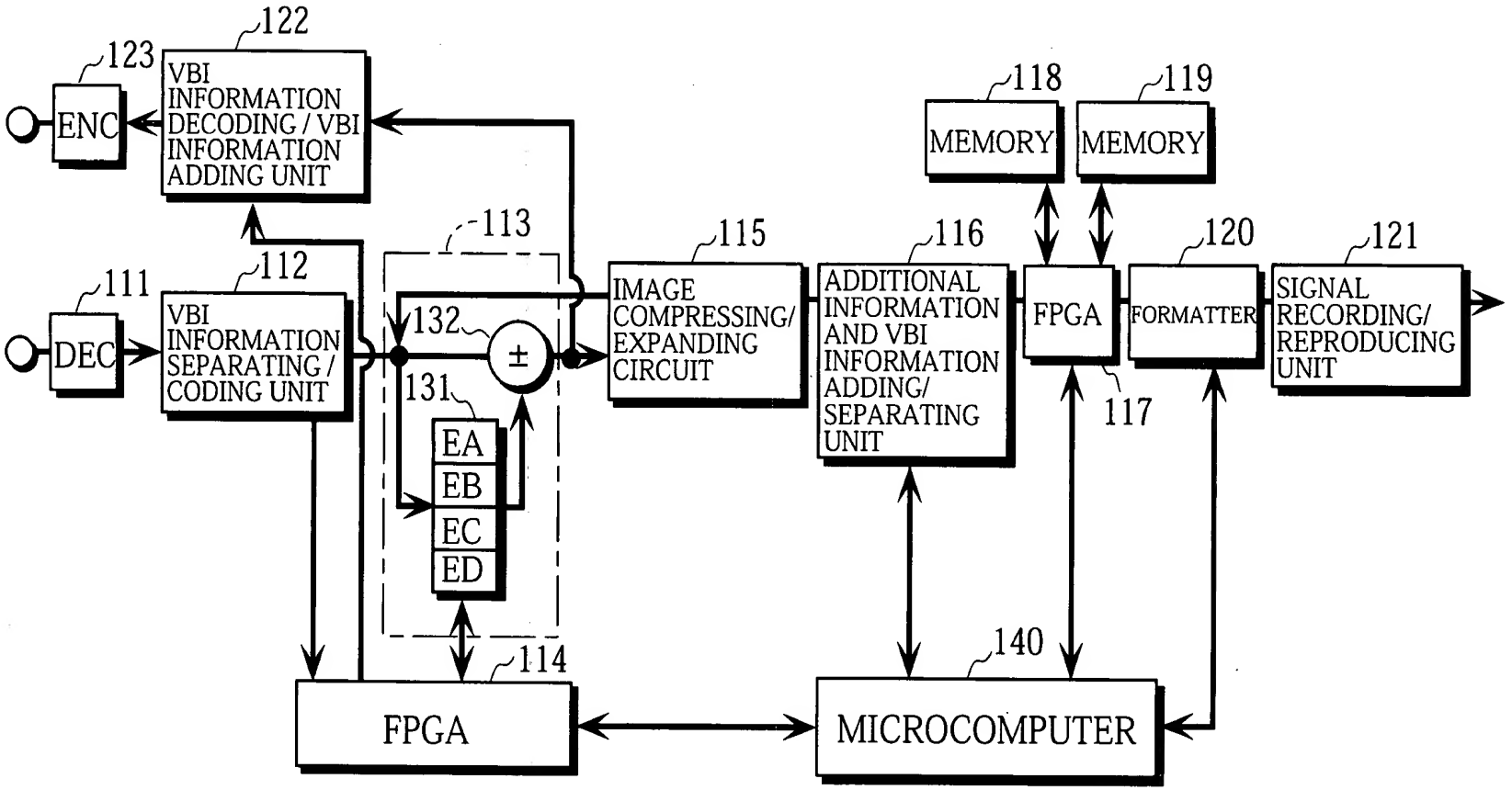

122
123
ENC
VBI INFORMATION DECODING / VBI INFORMATION ADDING UNIT
118
MEMORY
119
MEMORY
113
115
116
120
121
111
112
DEC
VBI INFORMATION SEPARATING / CODING UNIT
132
±
IMAGE COMPRESSING/ EXPANDING CIRCUIT
ADDITIONAL INFORMATION AND VBI INFORMATION ADDING/ SEPARATING UNIT
FPGA
FORMATTER
SIGNAL RECORDING/ REPRODUCING UNIT
131
EA
EB
EC
ED
117
114
140
FPGA
MICROCOMPUTER

FIG. 12a

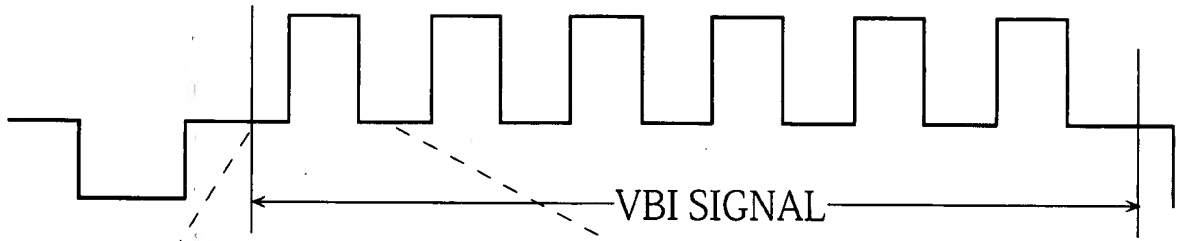


FIG. 12b

FIG. 12c

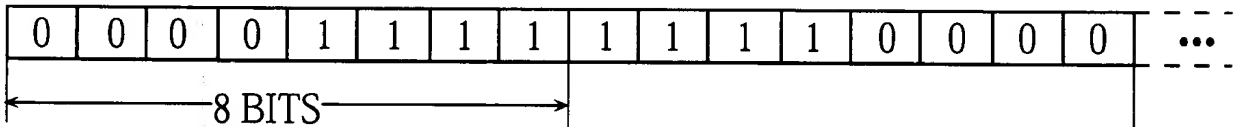


FIG. 12d

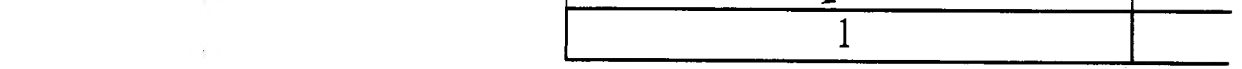


FIG. 13

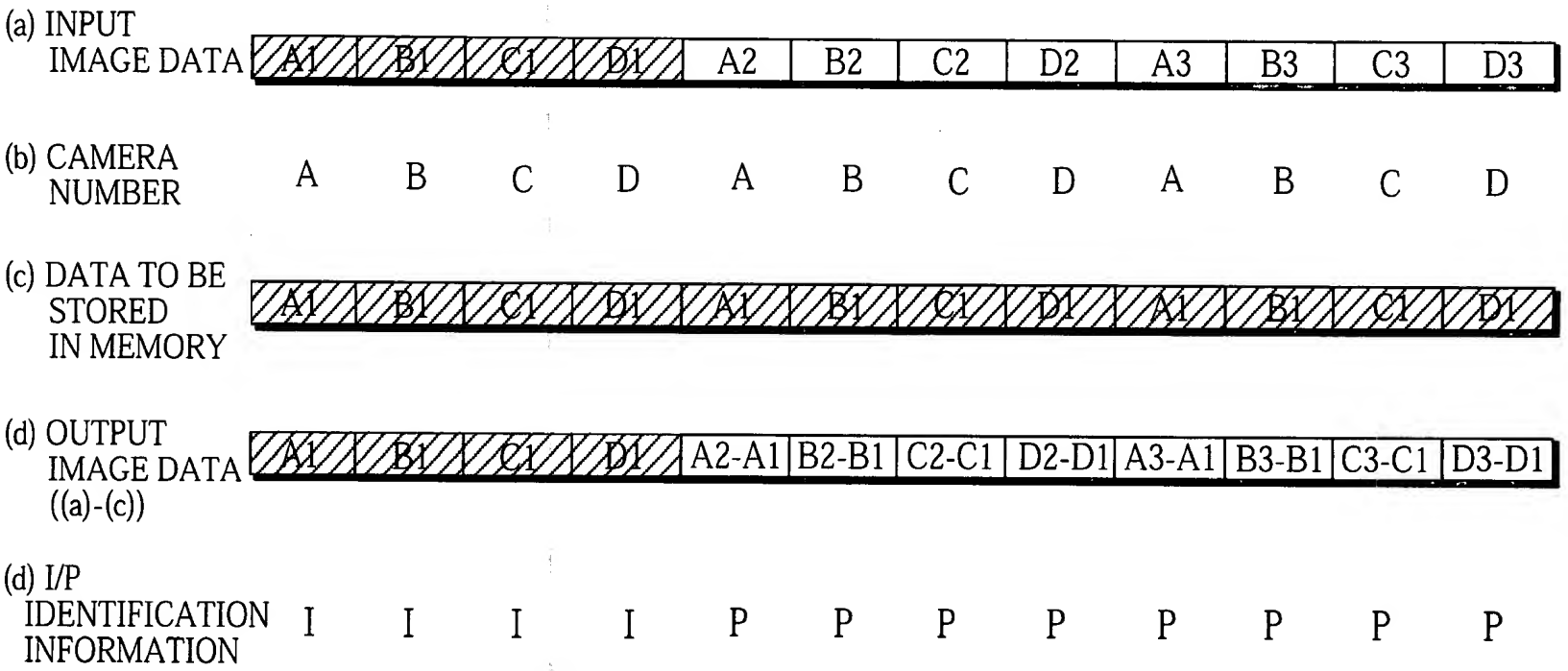

(a) INPUT IMAGE DATA
A1 B1 C1 D1 A2 B2 C2 D2 A3 B3 C3 D3
(b) CAMERA NUMBER
A B C D A B C D A B C D
(c) DATA TO BE STORED IN MEMORY
A1 B1 C1 D1 A1 B1 C1 D1 A1 B1 C1 D1
(d) OUTPUT IMAGE DATA ((a)-(c))
A1 B1 C1 D1 A2-A1 B2-B1 C2-C1 D2-D1 A3-A1 B3-B1 C3-C1 D3-D1
(d) I/P IDENTIFICATION INFORMATION
I I I I P P P P P P P P

FIG. 14

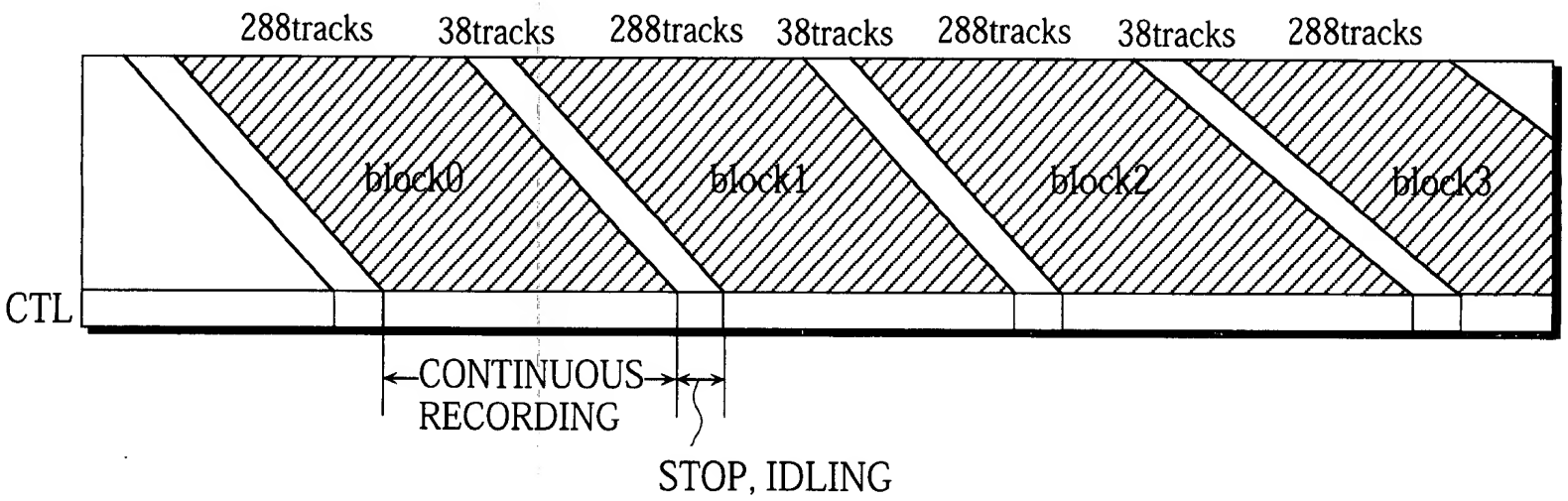

288tracks
38tracks
288tracks
38tracks
288tracks
38tracks
288tracks
block0
block1
block2
block3
CTL
CONTINUOUS
RECORDING
STOP, IDLING

FIG. 15

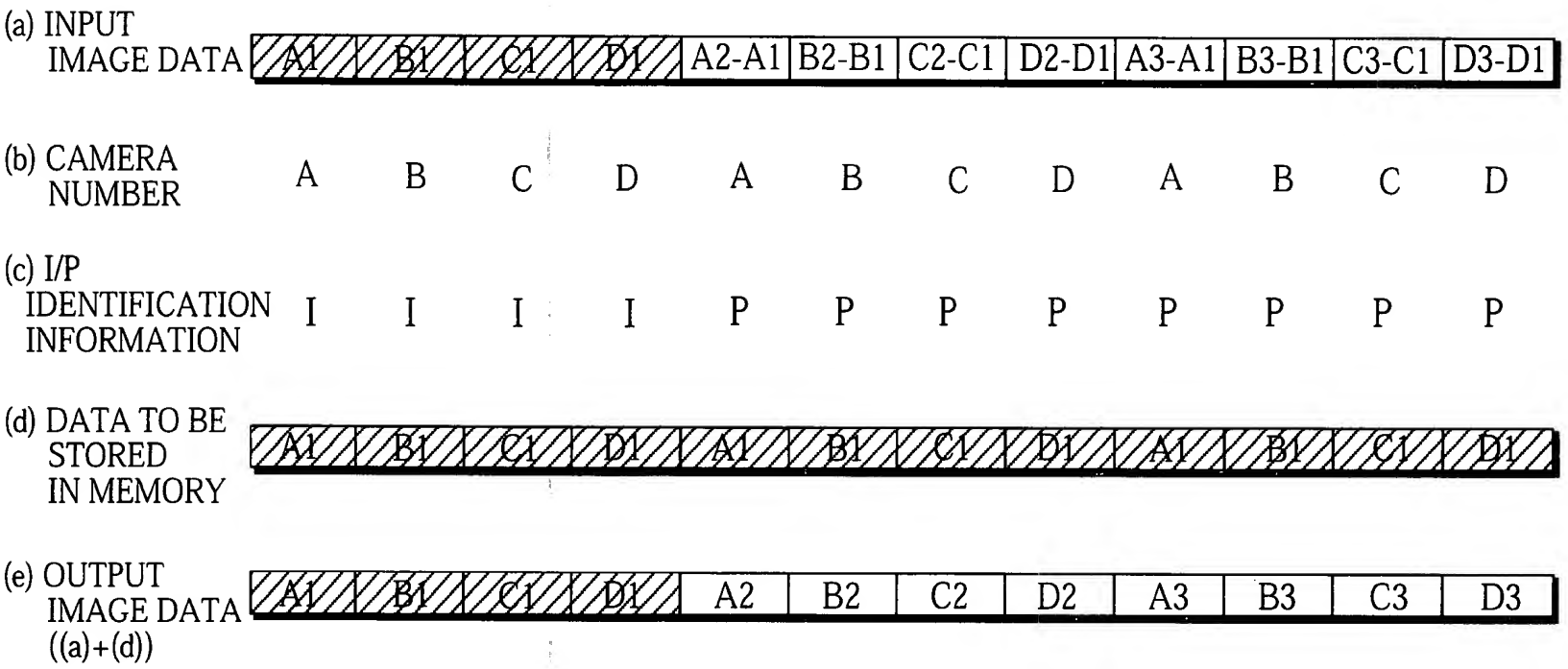
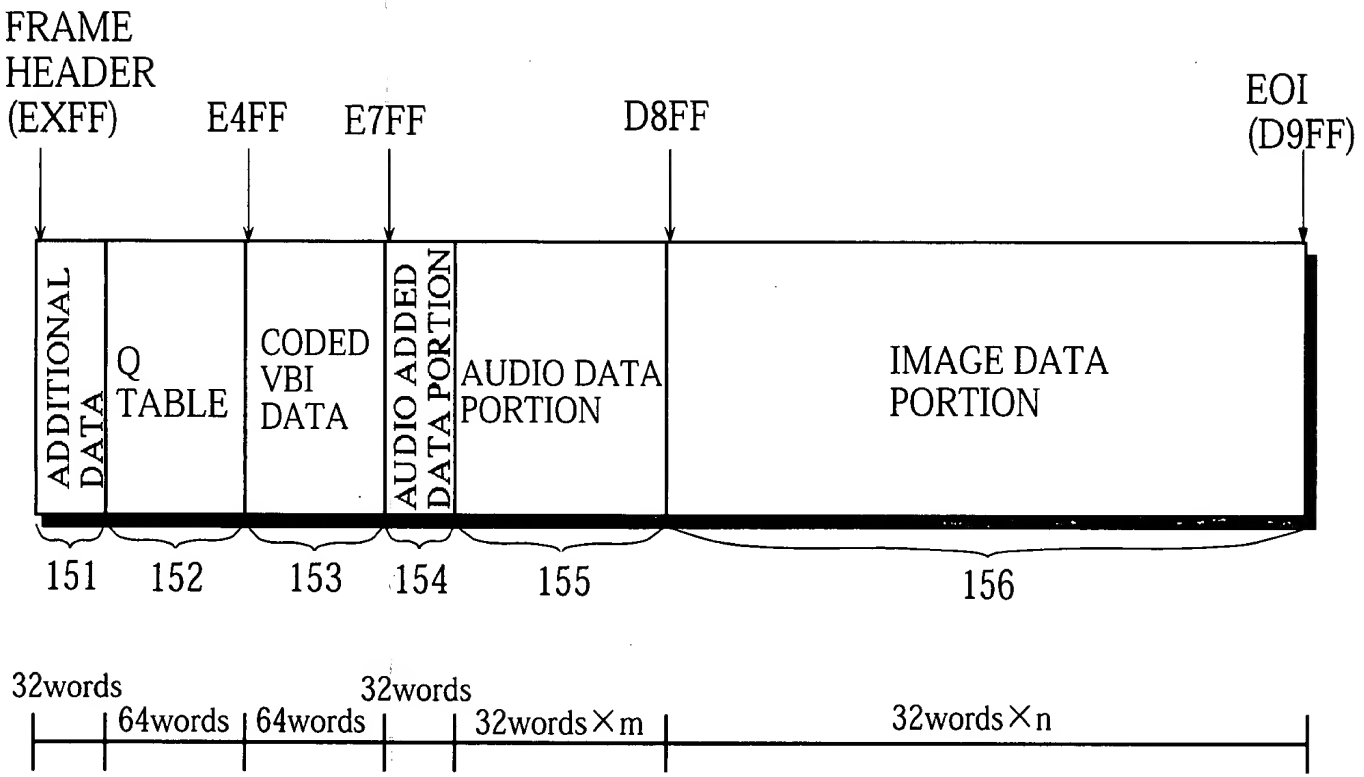

(a) INPUT IMAGE DATA
A1 B1 C1 D1 A2-A1 B2-B1 C2-C1 D2-D1 A3-A1 B3-B1 C3-C1 D3-D1
(b) CAMERA NUMBER
A B C D A B C D A B C D
(c) I/P IDENTIFICATION INFORMATION
I I I I P P P P P P P P
(d) DATA TO BE STORED IN MEMORY
A1 B1 C1 D1 A1 B1 C1 D1 A1 B1 C1 D1
(e) OUTPUT IMAGE DATA ((a)+(d))
A1 B1 C1 D1 A2 B2 C2 D2 A3 B3 C3 D3

FIG. 16


FRAME HEADER (EXFF)
E4FF
E7FF
D8FF
EOI (D9FF)
ADDITIONAL DATA
Q TABLE
CODED VBI DATA
AUDIO ADDED DATA PORTION
AUDIO DATA PORTION
IMAGE DATA PORTION
151
152
153
154
155
156
32words
64words
64words
32words
32words×m
32words×n